WHAT IS CLAIMED IS:

13, 17

1. A method of bonding the layers of a multi-layer semiconductor package comprising the steps of:

perforating at least a first layer with a plurality of vias;

aligning a second layer with the first layer such that the first layer has a surface adjoining and coplanar with a surface of the second layer; and

applying attach material between adjoining coplanar surfaces of the first and second layers and within the plurality of vias such that a bond is formed between the layers wherein the vias provide a bonding surface.

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2. The method of claim 1 further comprising the steps of coplanarly aligning at least one additional layer with the first or second layer; and

applying attach material between adjoining coplanar surfaces of the aligned first or second layers and at least one additional layers such that a bond is formed between the layers to form a multi-layer semiconductor package comprising three or more layers.

3. The method of claim 1 further comprising the step of perforating at least one additional layer with a plurality of vias.

4. The method of claim 1 wherein the perforating step further comprises the step of providing perforation substantially perpendicular to the plane of the perforated layer.

5. The method of claim 1 wherein the step of applying attach material further comprises the step of soldering.

6. The method of claim 1 wherein the step of applying attach material further comprises the step of epoxying.

7. The method of claim 1 wherein the step of applying attach material further comprises the step of flowing the attach material using a vacuum.

8. The method of claim 1 wherein the perforating steps further comprise the step of laser drilling.

9. The method of claim 1 further comprising the step of determining one or more uniform via interval prior to performing the perforating steps.

10. The method of claim 1 further comprising the step of determining one or more predicted stress point intervals prior to the perforating steps.

11. The method of claim 1 wherein the perforating steps further comprising the step of drilling.

12. The method of claim 1 wherein the perforating steps further comprising the step of etching.

13. A method of bonding the layers of a multi-layer semiconductor package comprising the steps of:

perforating at least a first layer with a plurality of vias;

applying attach material within the plurality of vias; and

aligning a second layer with the first layer such that the first layer has a surface adjoining and coplanar with a surface of the second layer;

whereby a bond is formed between the layers wherein the vias provide a bonding surface.

14. The method of bonding the layers of claim 13 wherein the step of applying attach material within the plurality of vias includes inserting solder material within the plurality of vias.

15. A method of bonding the layers of a multi-layer semiconductor package comprising the steps of:

perforating at least a first layer with a plurality of vias;

aligning a second layer with the first layer such that the first layer has a surface adjoining and coplanar with a surface of the second layer;

positioning a third layer against the first layer; and

applying attach material between adjoining coplanar surfaces of the first and second layers and within the plurality of vias such that a bond is formed between the layers wherein the vias provide bonding surface, the third layer providing a guide for correct placement of the attach material.

16. The method of method of bonding the layers of a multi-layer semiconductor package of claim 15 further comprising, after the step of applying attach material between adjoining coplanar surfaces, the step of removing the temporary layer.

17. A method of bonding the layers of a multi-layer semiconductor package comprising the steps of:

perforating at least a first layer with a plurality of vias;

aligning a second layer with the first layer such that the first layer has a surface adjoining and coplanar with a surface of the second layer; and

applying a material between adjoining coplanar surfaces of the first and second layers and within the plurality of vias.

18. The method of claim 17 wherein the material forming between the surfaces of the first and second layers provide thermal conduction of the semiconductor package.

19. The method of claim 17 wherein the material forming between the surfaces of the first and second layers provide electrical conduction of the semiconductor package.

20. The method of claim 17 wherein the material forming between the surfaces of the first and second layers provides a dielectric for the semiconductor package.